The VME Timing Module V3.0
Brief Description

The VTM is a 9U x 400mm VME board. It resides in the VME Readout Crate. The primary purpose of the module is to control the formation of Time Blocks of data on the MASTER Module, and to control the readout of the buffers. This is accomplished as follows:

The DAQ system collects fragments of data from the entire detector. The fragments are grouped into intervals of time called Time Blocks. This is done so that the software trigger can process the data that it receives efficiently. The Time Blocks are formed by controlling the length of time that a particular buffer on each MASTER Module is active for writing.

The control of the readout buffers is implemented by the VTM. The module receives the programmable Time Block Marker signal from the Master Clock Fanout module, and uses it to generate VME Interrupt Requests. The Interrupt Requests are sent across the backplane of the VME crate. The MASTER Modules in the crate "spy" on the Interrupt Request signals, and use them to change state of the buffers. The VME Processor also receives the Interrupt Requests, and uses them to initiate a new cycle for reading data from the buffers.

There are two readout buffers on each MASTER Module, and they may be located at different logical VME addresses. It is desirable for the buffer state to be synchronized across the entire crate, so that the VME Processor knows where in address space to read the data for a given Time Block period. To achieve this, the VTM uses two VME Interrupt signals IRQ4, and IRQ3 , one for each buffer. Each Interrupt Request is asserted in alternating fashion, for example: first Interrupt A, then Interrupt B, then Interrupt A, etc. In this way, a particular readout buffer, along with its VME address space, are associated with a particular Interrupt Request. The convention shall be that the assertion of a particular Interrupt Request causes the associated buffer to be put into the "Read" state, with the other buffer put into the "Write" state. Each MASTER Module handles the control of its own buffers based on this convention.

The Time Block Marker signal from the Master Clock is programmable at the system level. It is a periodic signal, except for a special consideration described below. The nominal period is expected to be approximately 50 mS, with a range of 1 mS to 255 mS, in 1 mS steps (8 bits.) This is used to form Time Blocks of data across the entire system.

The Time Block Marker signal is fanned out to all VME Crates in the system simultaneously, so that readout buffers on MASTER Modules change state at the same time. Due to propagation delays, there may be an uncertainty in exactly when a buffer changes state on a given MASTER Module. The uncertainty is on the order of 200 nS across the entire system. The buffers do not change state in such a way as to cause data from a spill to be split between buffers (see below), so this uncertainty affects only data from cosmic rays. The Trigger and DAQ shall ensure that there is sufficient overlap of data fragments at the edges of Time Blocks, so that the loss of efficiency in triggering due to edge effects is reduced.

A second function of the VTM is to provide the system clock for the MASTER Modules. This is accomplished by receiving QCLK from the Master

Clock Fanout , and by dividing the frequency by a factor of two to generate SYSCLK. This is then sent onto the backplane of the VME crate. SYSCLK is received by the MASTER Modules, and is used to process incoming data. Since the MINDER Modules transfer data at this frequency, the MASTER may not process the data at a faster rate. The divide-by-two circuitry is easily implemented with Phase-Lock-Loop components.

A third function of the VTM is to record real-time information from the GPS system, and make it available to the VME Processor. To accomplish this, the VTM receives signals from the GPS system, and the Spill Gate. The VTM latches the GPS information in coincidence with the leading edge of the Spill Gate, creating a real-time timestamp for the start of the spill. This information can then be read out as part of the spill data, and provides a means of correlating events from the spill between the Near and Far Detectors. It is desirable for the VTM to provide information that correlates the time of QCLK with the GPS time. To accomplish this, the VTM has a timing circuit that is identical to that used on the front end boards. This circuit is a counter, which is cleared by CNTRST and advances with every QCLK. The value of the counter is latched and is stored in a register at the leading edge of the Spill Gate signal. When the GPS information is read as part of the data from the spill, the time of the spill is recorded and made available to the data acquisition system.

The VTM has a VME interface, so that the VME Processor can read out the spill information

Input Signals
The VTM receives the following signals as inputs to the system:
1. Time Block Marker (TBMKR)
The TBMKR is received from the Master Clock. It is received as encoded PECL
        Via HotLink Chip set.
2. QIE Clock (QCLK)
QCLK is received from the Master Clock. It is received as encoded PECL
Via HotLink Chip set.
3. Spill Gate (SGATE)
The Spill Gate signal is received from the Master Clock. It is received as
encoded PECL Via HotLink Chip set.
4. Counter Reset (CNTRST)
The Counter Reset signal is received from the Master Clock. It is received as
encoded PECL Via HotLink Chip set.
5. Pulse per Second from GPS system (GPS_PPS)
Timing signal received from the GPS Fanout. It is received as LVDS.
6. Clock from GPS system (GPS_CLK)
10 MHz clock received from the GPS Fanout. It is received as LVDS.

Output Signals
The VTM generates the following signals in response to the Input Signals:
1. VME Interrupt Requests
The VTM receives the Time Block Marker from the Master Clock. In
response, it generates one of two VME Interrupts; IRQ4 and IRQ3. The VTM
alternates between the two interrupts as it receives subsequent the TBMKR signal from
the Master Clock.
2. System Clock (SYSCLK)
The VTM receives QCLK from the Master Clock, and divides the frequency
by 2 to generate SYSCLK. This is sent onto the VME backplane, using SERA pin.

Switch and Jumper settings

VME base address selection is controlled by dip switches, chip #'s U14 and U12. U14segment 8-1 control VME address bits A31-A24, and U12 segment 1-8 control VME address bits A23-A16. Turning a segment to the on position sets the address bit being compared to low.

Jumper J7 selects the mode of operation for the VTM module. Removing the jumper Puts the VTM into local mode. In local mode the VTM ignores the control signals coming from the Master Clock Module, and generates these signals locally. The frequency of the control signals can be modified by reprogramming the pal chips. . When the VTM is placed into local mode, a red LED turns on to warn the user that the VTM is no longer in normal data taking mode.

Jumper J-RF is used to select the source of RF Clock. If the jumper is shorting the upper two pins RF/2 is taken from the local oscillator. If the jumper is shorting the lower two pins RF/2 is taken from the HotLink Chip (decoded from the Master Clock System).

Jumper J-GPS is used to select the source of the 10 Mhz GPS Clock. If the jumper is shorting the upper two pins GPS Clock is taken from the local oscillator. If the jumper is shorting the lower two pins GPS Clock is taken from the GPS Fanout.

Jumper Block J8 is used to select the Interrupt request mode. Removing the jumper puts the VTM into Interrupt Request Self Reset mode. In this mode the VTM asserts and then releases the VME interrupt request lines without waiting for a Interrupt acknowledge cycle from the processor. When the VTM is placed into this mode, a red LED turns on to warn the user that the VTM is no longer in normal data taking mode.

Jumper Block J9 is used to select the SYSCLK drive option. Removing the jumper disables the SYSCLK driver chip. For normal operation this jumper must always be installed.

Interface to the Experiment
The VTM has a normal VME interface, so that it can be read by the
VME processor. The following information is provided by the VTM through the
VME interface:

VME D32 READABLE REGISTERS
 OFFSET   FUNCTION
 0x00   Read GPS Counter Register Latched by SGATE
            (persists until next TBMKR)
d 0x04   Read GPS Counter Register Latched by SGATE
 0x08   Read GPS Counter Value Latched by CNTRST
            (persists until next TBMKR)
d 0x0c   Read GPS Counter Value Latched by CNTRST
d 0x10   Read TBMKR counter
 0x18   Read Value of TBMKR counter at CNTRST
            (persists until next TBMKR)
d 0x1c   Read Value of IACK counter at CNTRST
            (persists until next TBMKR)
d 0x30   Read Interrupt/Iack difference counter
d 0x34   Read Value of CNTRST counter

(persists until next TBMKR)

0x40		Read RF Counter Register Latched by SGATE
		(persists until next TBMKR)
d 0x44		Read RF Counter Register Latched by SGATE
d 0x48		Read RF Counter Register Latched by TBMKR
0x50		Read Value of RF counter Latched by CNTRST
		(persists until next TBMKR)
d 0x54		Read Value of RF counter Latched by CNTRST
d 0x74		Read IRQ4 vector
d 0x78		Read IRQ3 vector
d 0x84		Read CSR0 register
d 0x88		Read Test i/o register

VME D32 WRITABLE REGISTERS

OFFSET	DATA	FUNCTION
d 0x20	0	Force Reset of GPS Counter
d 0x24	0	Force Reset of RF Counter
d 0x28	0	Force Latch of RF Counter Register Latched by TBMKR, also assert IRQ on backplane if none active
d 0x2c	0	Force Latch of RF Counter Register Latched by SGATE
d 0x50	0	Force Latch of RF Offset Register Latched by SGATE
d 0x60	0	Turn on VME interrupts
d 0x64	0	Turn off VME interrupts
0x68	0	RESET Pending IRQ and RESET Pointer to IRQ 4
d 0x6c	0	RESET Pointer to IRQ 4
0x70	0	Send FPGA Reload Command to MASTER MODULES and VTM FPGA
d 0x74	8 bit #	Overwrite default IRQ4 vector
d 0x78	8 bit #	Overwrite default IRQ3 vector
0x7c	0	RESET VTM
d 0x84	8 bit #	Write to CSR0 register
d 0x88	32 bit #	Write to Test i/o register

d == debug feature (not needed for DAQ running)

Brief description taken from "Conceptual Design of The Clock System for The MINOS Near Detector"
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Version 2.1
July 25, 2000